REMARKS

Claim 1 is amended. Claims 1-13 remain for consideration. The allowability of claims 7-8 is acknowledged. All remaining claims are thought to be allowable over the cited art.

The Office Action fails to establish that claims 1-6 and 9-13 are anticipated under 35 U.S.C. §102(b) by U.S. Patent No. 5,398,263 to Vanderspool II et al. (hereinafter Vanderspool). Applicants have, nevertheless, amended claim 1 in order to advance prosecution.

Applicants' claim 1 at least sets forth selectable coarse and fine loop phase-locked loops (PLLs), where the selectable coarse loop PLL "[produces] a coarse loop synchronized oscillation signal based on a reference clock," e.g., reference clock 238 of FIG. 8 of the instant application, and the selectable fine loop PLL "[adjusts] the coarse loop synchronized oscillation signal in phase coherence with the received high data rate serial data," e.g., inbound serial data 52 of FIG. 8 of the instant application. Thus, the coarse loop synchronized oscillation signal of Applicants' claim 1 is first adjusted based on a reference clock signal and is subsequently adjusted to be in phase coherence with the input serial data.

Vanderspool, on the other hand, seems to teach that both the coarse adjustment and the fine adjustment are performed in phase coherence with a reference clock signal and that neither adjustment is performed in phase coherence with the input serial data, which is in contradistinction to Applicants' claim 1. In particular, Vanderspool seems to teach that the phase comparator of FIGs. 7, 8, and 10, receives as input: the bit clock, the incoming clock signal, the sample clock, and the 1 PPS signal. (See column 7, lines 62-64). Vanderspool further seems to teach that: the bit clock is derived by divider 521 by dividing a 16.8 MHz clock reference by 21; the incoming clock signal is equal to the 16.8 MHz clock reference; the sample clock is derived by dividers 523 and 525, which divide the bit clock signal by successive integer divisions of 2 and 8, respectively; and the 1 PPS signal is a one pulse per second signal. (See column 6 line 59 to column 7 line 13.)

Thus, since Vanderspool's phase comparator does not receive the input serial data as one of its inputs, it seems to follow that Vanderspool's phase comparator

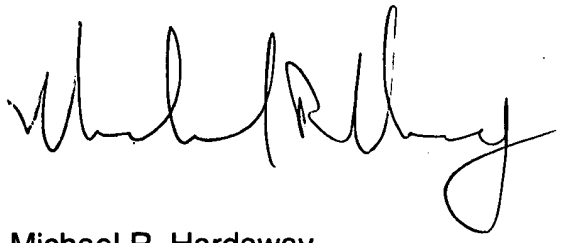
cannot adjust the phase of any of its clock signal inputs to the phase of the input serial data. Further, Vanderspool teaches that the function of the phase comparator is to "[measure] the number of incoming clock signals difference from the rising edge of the 1 PPS signal to the rising edge of the sample clock." (See column 8, lines 15-18). Vanderspool further seems to teach that the sample clock may be advanced or retarded by the phase comparator based upon the number of incoming clock signals that are measured between the rising edge of the 1 PPS signal and the rising edge of the sample clock. (See column 8, lines 18-38). Thus, it seems that Vanderspool's coarse and fine phase adjustments are effected without regard to the phase of the input serial data, which is in contradistinction to Applicants' claim 1. Applicants respectfully submit, therefore, that claim 1 patentably distinguishes over Vanderspool and is in condition for allowance.

Dependent claims 2-6 and 9-13, which are dependent from independent claim 1, are also rejected under 35 U.S.C. §102(b) as being unpatentable over Vanderspool. While Applicant does not acquiesce to the particular rejections of these dependent claims, it is believed that these rejections are now moot in view of the remarks made in connection with independent claim 1. These dependent claims include all of the limitations of the base claim and any intervening claims, and recite additional features which further distinguish these claims from the cited references. Therefore, dependent claims 2-6 and 9-13 are also in condition for allowance.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the amendments and remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on December 7, 2006.

Pat Tompkins — *Name*

Signature